Amendments to the Specification:

Please replace paragraph **7** with the following amended paragraph:

[07] Conventional high-density mask ROM devices employ various flat-cell array layouts. Such array includes a plurality of buried N-doped (BN+) or P-doped (PN+) parallel bit-lines into silicon and a plurality of polysilicon/oxide word-lines fabricated on a top surface of the silicon perpendicular to the bit-lines. The set of BN+ or BP+ strips and set of polysilicon ~~world~~ word lines are often important elements of each individual MOS device unit corresponding to one memory cell. Such elements also serve as local electronic interconnections for the memory cells to their peripheral outlets. To reduce wafer production costs, polysilicon gate/word lines are manufactured at the same time with the polysilicon gates for CMOS devices used in the periphery portion of the mask ROM. Unfortunately, such high-density ROM devices also suffer from many drawbacks. Here, shorting may occur between adjacent bit-lines. Additionally, such conventional devices also have parasitic problems when scaling down to smaller and smaller design rules. These and other limitations are described throughout the present specification and more particularly below.

Please replace paragraph **14** with the following amended paragraph:

[14] Figure 1 is a simplified top-view diagram of a ROM memory device in an array and a simplified circuit diagram of the ROM memory device according to an embodiment of the present invention;

Please replace paragraph **20** with the following amended paragraph:

[20] Figure 1 is a simplified top-view diagram of a memory device 100 in an array and a simplified circuit diagram 110 of the memory device according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the top view diagram of the device is provided for a memory array region. The memory array region includes a plurality of memory cells. Each of the memory cells 107 includes a read only memory ("ROM") device, but can also be others. A

peripheral region 109 is also included. The peripheral region includes logic circuitry, input/output drivers, sense amplifiers, and other devices. The peripheral region can also include sub-system devices, such as processing devices, e.g., digital signal processing, microprocessor, and micro-controller devices. The array region includes a plurality of trench isolation regions 101, which separate each of the cells from each other. The array region also includes a plurality of polysilicon word lines 103, which run along a first direction in parallel to each other. The array region also includes a plurality of bit lines 105, which are buried regions. Each of the bit lines also couple to source/drain regions for each of the memory devices.

Please replace paragraph **21** with the following amended paragraph:

[21] Figure 2 is a simplified top-view diagram of a memory device 200 in an array according to an alternative embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in Figure 2 as some of the other Figures described herein. Such reference numerals are not intended to be limiting in any manner, but are provided for cross-referencing purposes only. As shown, the top view diagram of the device is provided for the memory array region. The memory array region includes the plurality of memory cells, which are isolated from each other. Each of the memory cells 107 includes the read only memory ("ROM") device, but can also be others. As shown is the peripheral region 109. The peripheral region includes logic circuitry, input/output drivers, sense amplifiers, and other devices. The peripheral region can also include sub-system devices, such as processing devices, e.g., digital signal processing, microprocessor, micro-controller devices. The array region includes the plurality of trench isolation regions 101, which separate each of the cells from each other. The array region also includes the plurality of polysilicon word lines 103, which run along a first direction in parallel to each other. The array region also includes the plurality of bit lines 105, which are buried regions. Each of the bit lines also couple to source/drain regions for each of the memory devices. A sidewall spacer 201 is formed adjacent to the polysilicon word line. The top portion of the word line and top portion of the bit line include refractory metal, which reduces a resistance value of the word line and the bit

line. The refractory metal layer can include a titanium silicide layer, a tungsten silicide layer, any combination of these, and others. Cross-sectional view diagrams of the array region are provided below, where cross-sections ~~between Y and~~ Y2-Y2 ~~and Y~~ and Y1-Y1 are shown.

Please replace paragraph **22** with the following amended paragraph:

[22] Figure 3 is a simplified cross-sectional view diagram of a cell array of Figure 2 according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in Figure 3 as some of the other Figures described herein. As shown, the cross-sectional view ~~is between Y and~~ Y1-Y1, which is across the bit line structure 105 within substrate 301. The side-view diagram includes word line 103, which overlies dielectric layer 309. The dielectric layer is a gate dielectric layer. Such gate dielectric layer can include silicon dioxide, silicon nitride, any combination of these and the like. The buried bit line 105 is also included. Sidewall spacers 201 are formed using conventional processes adjacent to the word line structure. A refractory metal layer 305 is formed overlying the top of the word line. A refractory metal layer 307 is also formed overlying the exposed portion of the buried bit line, which also serves as source/drain region. The refractory metal overlying the buried bit line reduces a resistance value of the buried bit line. A further cross-section of the array structure is provided below.

Please replace paragraph **23** with the following amended paragraph:

[23] Figure 4 is a simplified cross-sectional view diagram of a cell array of Figure 2 according to an alternative embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in Figure 4 as some of the other Figures described herein. As shown, the cross-sectional view ~~is between Y2 and~~ Y2-Y2~~,~~ are across the trench isolation structure. The side-view diagram includes word line 103, which overlies dielectric layer 309. The dielectric layer is a gate dielectric layer. Such gate dielectric layer can include silicon dioxide, silicon nitride, any combination of these and the like. The buried bit line 105 is ~~also~~ not shown ~~included~~. Sidewall

spacers 201 are formed using conventional processes adjacent to the word line structure. The sidewall spacer includes a portion that is formed overlying a portion of the trench region. A refractory metal layer 305 is formed overlying the top of the word line. A top portion 401 of the trench region 101 is substantially free from any conductive layer such as the refractory metal layer. Accordingly, a first memory cell region ~~401~~ 403 is isolated from a second memory cell region ~~403~~ 405 by way of the trench isolation 101, which is provided between each of these cell regions. The trench isolation region is formed to a depth below the buried bit line region. Further details of the present invention are provided below.